EPC eGaN® FETs Reliability Testing: Phase 9

Chris Jakubiec, Rob Strittmatter Ph.D., and Chunhua Zhou Ph.D. Efficient Power Conversion Corporation, El Segundo, CA

The continued adoption of Efficient Power Conversion (EPC) Corporation's eGaN® devices necessitates additional reliability data to prove capability over many applications. The Phase 9 reliability report adds to the growing knowledge base that has been previously published in EPC's first eight reports. The main section of this report covers thermo-mechanical board level reliability, focusing on a predictive model for solder joint integrity. Appendix A provides details of the method to calculate solder joint strain energy density during thermal cycling, as is referenced in the report. Appendix B contains cumulative product specific stress test data from previously published reliability reports, as well as data collected after the Phase 8 report was released.

THERMO-MECHANICAL STRESS MODEL

Thermo-mechanical reliability, focusing on Wafer Level Chip-Scale (WLCSP) package to printed circuit board (PCB) solder joint interface integrity, was introduced in the Phase 7 and Phase 8 reports. This report extends the initial thermal stress cycles to solder joint fatigue failure model by including several die sizes, package footprints, and stress conditions for validation.

Wafer Level Chip-Scale Solder Joint Integrity

EPC FETs and ICs are made in wafer level chip-scale packages to minimize board real estate while offering excellent thermal dissipation. Temperature variations, due to normal circuit operation and surrounding ambient conditions, result in stress on the solder joints between the die and the PCB assembly. The coefficient of thermal expansion (CTE) mismatch between the die (~2.6 ppm/°C) and PCB (~17 ppm/°C) [1], generates a strain energy that is mainly absorbed by the solder joints of the WLCSP package. Cyclic temperature variations over time fatigue the solder joints until they ultimately fracture and fail. All surface mount soldered components are susceptible to the stress related effects of accumulated temperature variation. The component size, stiffness, solder layout, and solder joint standoff height will all influence the ability of the device to withstand the thermo-mechanical stresses.

Experiment Overview

The experiment to determine stress related effects was extended by analyzing multiple EPC WLCSP devices. Three devices which span package size and solder layout configurations were selected. The device test set included a 2.05 mm x 0.85 mm Land Grid Array (LGA) package, a large 4.6 mm x 2.6 mm Ball Grid Array (BGA), and a very small 0.9 mm x 0.9 mm BGA package (see figures 1 - 3). The intention was to use accelerated temperature cycle testing until the solder joints started failing, and in parallel, calculate the accumulated strain energy at the joints due to the temperature swings. Thus, a predictive model was generated for expected number of thermal cycles to failure versus calculated solder joint strain energy density.

The solder joints were thermo-mechanically stressed by way of the Intermittent Operating Life (IOL) test. IOL is a variant of power cycle testing, where device self-heating is achieved by applying a constant power within a targeted time interval. In the case of EPC Field Effect Transistors (FETs), the devices are biased in a linear-mode in order for the junction temperature (Tj) to reach a predefined level. A circuit with a feedback control loop at the gate of the FET, is used to ensure the same power is applied to all devices (figure 4). The heating phase is then followed by a cool-down phase

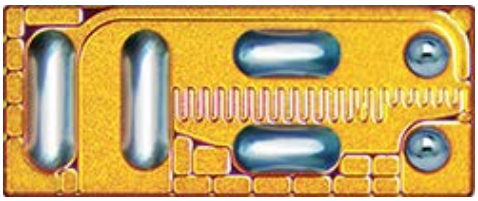


Figure 1. 2.05 mm x 0.85 mm land grid array WLCSP package.

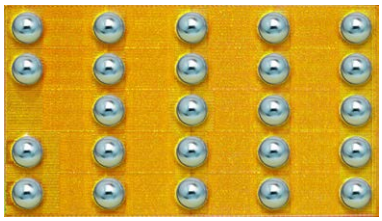


Figure 2. 4.6 mm x 2.6 mm ball grid array WLCSP package.

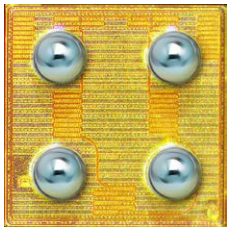


Figure 3. 0.9 mm x 0.9 mm ball grid array WLCSP package.

by removing the applied power and allowing the device to reach the lower temperature target. The lower Tj value is often set to ambient room temperature, however it can also be adjusted to simulate specific circuit applications. Forced air is used in the cooling phase to speed the temperature transition. The test devices are solder mounted on individual printed circuit board coupons. A FLIR thermal camera is used for temperature calibration and monitoring of the devices during the IOL testing. Figure 5 shows a thermal camera image of devices undergoing IOL stress test.

The device samples were subjected to parametric testing at predefined IOL intervals to check the DC datasheet specifications. A typical solder joint fracture failure results in an increased on-state ($R_{DS(on)}$) resistance as detected in parametric testing. For this experiment, an increase in $R_{DS(on)}$ of at least 10% was considered a failed device (see figure 7 example). Device package parameters such as solder joint standoff height were taken on samples from the test lots to provide accurate inputs to the model.

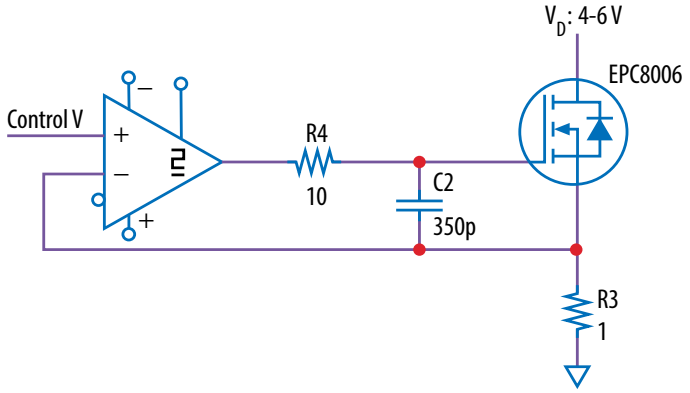


Figure 4. IOL test circuit – gate control loop used to provide same power to all devices.

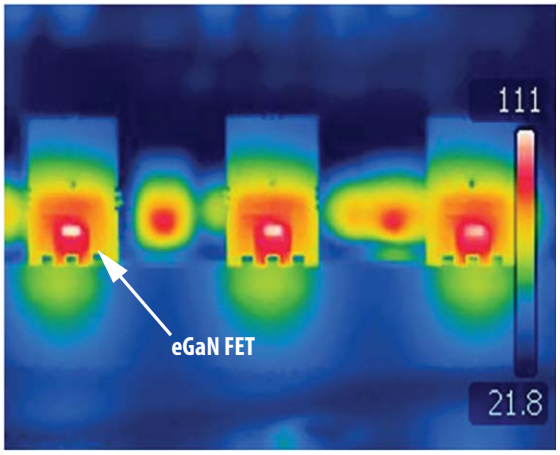


Figure 5. FLIR thermal camera image during IOL test – devices mounted to PCB coupons.

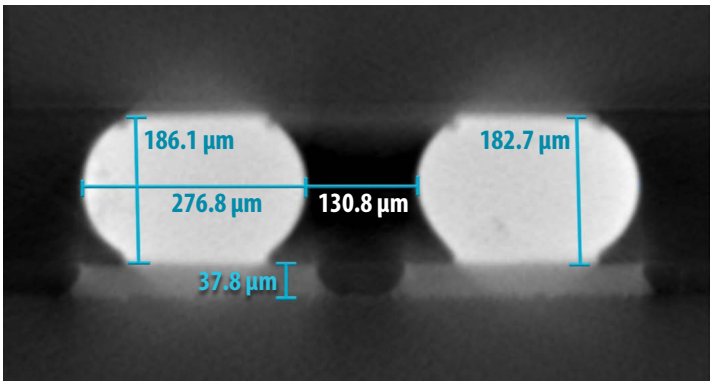


Figure 6. 3D X-ray Image – Test lot sample with measurements.

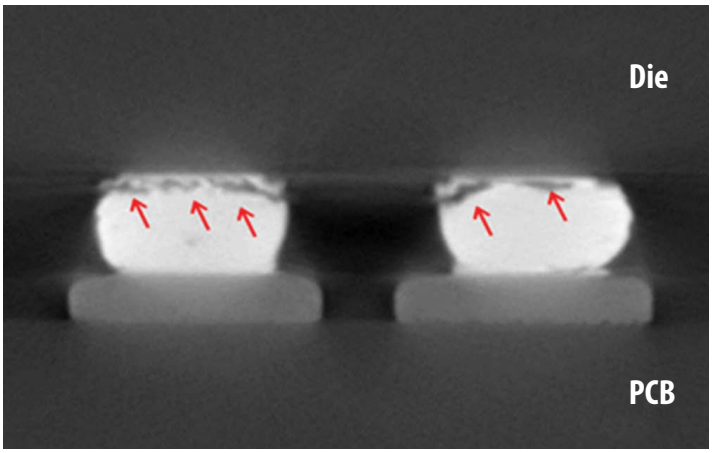


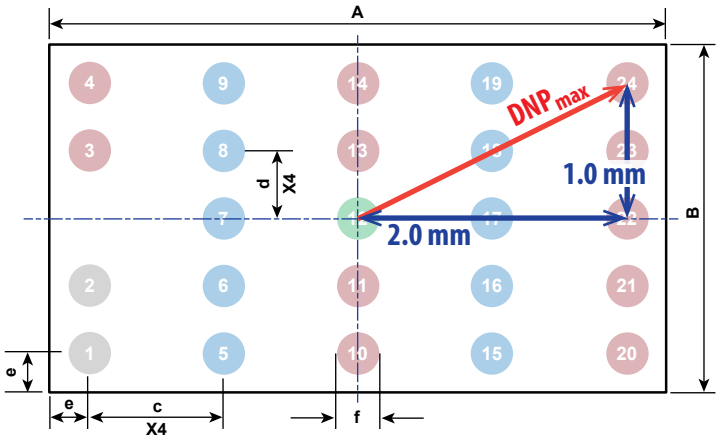
Figure 7. 3D X-ray Image – Solder joint fatigue failure from IOL test.

Solder Joint Strain Energy Density

Cyclic solder joint strain energy density was calculated using the methodology described by Clech in [26][27]. This algorithm calculates the combined stress and strain in the solder during a temperature cycle; the area inside the hysteresis loop is the cyclic strain energy density. This time-stepping method allows for a temperature vs. time profile of any arbitrary shape. For our calculations, the actual temperature profile was measured using a pyrometer and data-logger; the waveform was then input directly into the hysteresis loop simulator.

During a temperature change, stress builds up in the solder joint. The stress is of two principal types: global mismatch stress and local mismatch stress. The global stress is caused by the differential CTE of the component and PCB, leading to a mainly shear stress in the joint. The magnitude of this stress is determined by the height of the joint, as well as its distance from the neutral point of the assembly. The local stress is caused by the difference in CTE between the solder (~22 ppm/°C), component (~2.6 ppm/°C) and PCB (~17 ppm/°C) [1]. This local mismatch leads to both biaxial and shear stress in the joint. In this study, both the global and local strain energies were computed.

In Clech's approach, thermo-mechanical stress in the solder joint is relieved through one of three mechanisms: (i) elastic strain deformation; (ii) compliance of the rest of the assembly (component or PCB); or (iii) creep deformation of the solder. The compliance of the assembly is calculated, resulting in a net assembly stiffness parameter K. For the global mismatch



DIM	Micrometers		
	MIN	Nominal	MAX
A	4570	4600	4630
B	2570	2600	2630
c	1000	1000	1000
d	500	500	500
e	285	300	315
f	332	369	406

Figure 8. Distance to Neutral Point (DNP) – EPC2032 BGA.

case in this study, the solder joint farthest from the neutral point on the die was simulated. This is the joint with highest shear strain, and is most likely to fail first. For the local mismatch case, the location of the joint is not significant. Figure 8 shows an example of the solder joint calculated furthest distance to the neutral point (DNP).

Clech's approach was originally intended to model temperature cycling (TC), where the component and PCB are always at the same temperature. In IOL testing, the PCB will be at a lower temperature, depending on the thermal resistance junction-to-board ($R_{\theta JB}$), and the power being dissipated in the device. This has the effect of reducing the shear stress in the joints slightly compared to TC. To account for this condition, Clech's approach was adapted by computing an effective temperature, linearly related to the true case temperature, which accounts for differences in component and board temperatures during IOL testing. This adaptation is valid for the global mismatch case, but is of dubious validity for the local case, where full finite element modeling may be the only means to obtain realistic stress-strain fields in the joint.

Appendix A provides a complete listing of the equations, parameters, and models used to implement Clech's strain energy calculation. The intent of Appendix A is to provide EPC customers the means to predict solder joint reliability in their end-use conditions. EPC can also provide MATLAB code with a full implementation of the algorithm to calculate the strain energy.

Figure 9 (a) shows a representative temperature vs. time profile for a 25°C to 150°C IOL stress leg. Note that temperature is measured on the backside case of the die. Figure 9 (b) shows simulated hysteresis loops for three separate IOL legs on the EPC2032. As can be seen, relaxation from creep deformation becomes strong in the stress range of 10 - 15 MPa. The area inside the loop gives the strain energy density.

The same procedure was repeated for all IOL legs included in this study. The results are tabulated in table 1. For the larger die (EPC800x and EPC2032), the strain energy is dominated by the global mismatch. As a result, IOL cycles to failure would be expected to improve as the joint stand-off height is increased. For the very small EPC2036, however, the local strain energy actually exceeds the global. In this regime, reliability can only be improved by changing solder type (e.g. lower CTE, lower creep rate).

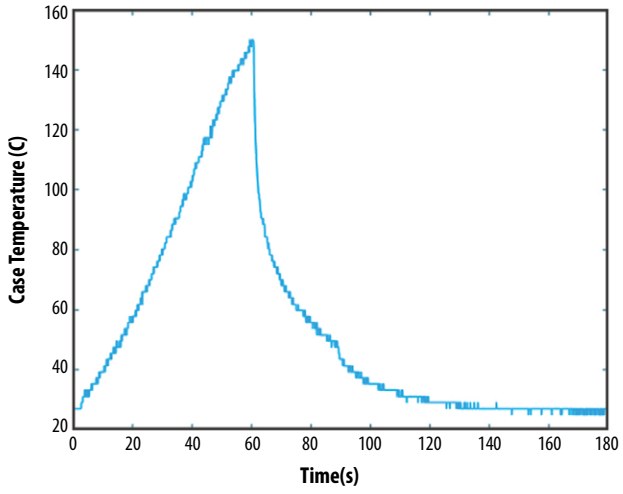


Figure 9 (a): Case temperature versus time for a typical IOL temp cycle (25°C to 150°C).

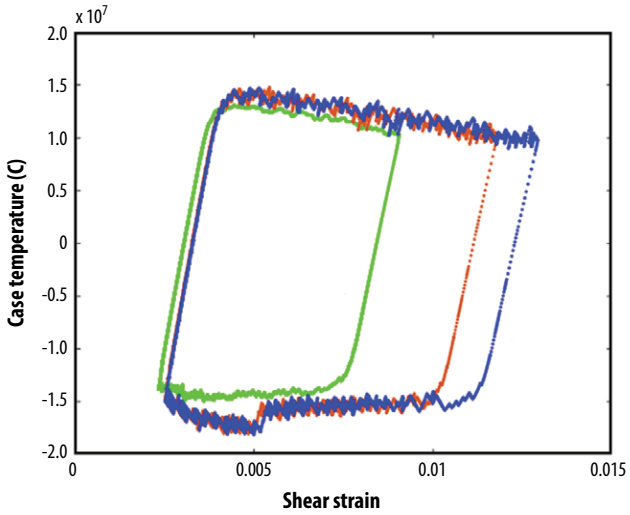


Figure 9 (b): Calculated shear stress-strain hysteresis loops for three different temperature ramp cycles. The area inside the loop gives the strain energy density.

Part Number	Waveform	Global Strain Energy Density (Mpa)	Local Strain Energy Density (Mpa)
EPC800x	25°C to 175°C	0.2043	0.0511
EPC800x	25°C to 163°C	0.158	0.0424
EPC800x	25°C to 150°C	0.1462	0.0358
EPC800x	25°C to 125°C	0.092	0.0305
EPC2032	40°C to 140°C	0.14	0.0192
EPC2032	25°C to 150°C	0.22	0.0278
EPC2032	25°C to 160°C	0.2493	0.0301
EPC2036	25°C to 150°C	0.0131	0.0274
EPC2036	25°C to 160°C	0.0154	0.0296
EPC2036	25°C to 175°C	0.0187	0.0328

Table 1. Calculated global and local strain energy densities for all IOL legs run in experiment.

In future iterations of this thermo-mechanical modeling, simulation of the local mismatch problem will be improved by incorporating finite element analysis (FEM) to calculate the stress-strain field inside the solder joint. This is especially helpful in the case where temperature gradients may exist between component and PCB. While FEM will be used to calculate the full 3D mechanical fields, the same basic time-stepping algorithm of Clech (coupled with the creep constitutive equation) can be used as before.

Thermo-Mechanical Stress Cycles to Failure Model

Numerous studies [22, 26, 27] have shown a strong correlation between strain energy density and cycles to failure for solder joints. The correlation is modeled as a simple power law. For BGA type packages, an exponent near -1 is typically found, meaning that the measure of cycles to failure is inversely proportional to strain energy.

Figure 10 shows N_{50} (cycles to 50% failure) versus strain energy density for all legs in this experiment. Device failures are defined against datasheet limits, and were tabulated at regular intervals during the total stress duration. In most cases, each leg was run until approximately half of the population had failed. From the cumulative failure versus stress cycles data, N_{50} was calculated using maximum likelihood estimation using a standard 2 parameter Weibull distribution. The error bars in figure 10 indicate 67% confidence intervals.

As can be seen in figure 10, two distinctly different correlation slopes (exponents) were found for the BGA (EPC2036 and EPC2032) versus the LGA (EPC800x) type packages. Equations for the actual best fit lines (solid lines) are provided in the figure. The dashed lines indicate ± 30% from the fit equation. For the BGA packages, the slope is near -1, in agreement with the bulk of the literature for BGA type packages. With the exception of one leg, all the data falls within a relatively tight band around the center line. For EPC800x, the measurements are also closely fit to the correlation equation, but the slope is steeper (exponent of -2). This package contains both circular and bar shaped solder joints. Thus, it is not surprising that the correlation is different as compared with BGA packages. Further data on LGA type devices will be collected to ascertain whether the steeper slope applies more generally.

Application of Model to Predict Thermo-Mechanical Reliability

Using the correlation between strain energy density and fatigue lifetime (discussed in the previous section), coupled with the ability to simulate strain energy for any arbitrary stress conditions, customers can make predictions/extrapolations about cycles to failure for their particular use cases. Examples of this type of analysis include:

- Lifetime versus peak temperature during cycle
- Lifetime versus temperature waveform (e.g. dwell time, ramp rate, cycle period)
- Lifetime under TC vs. IOL
- Lifetimes of different EPC devices

Figure 11 shows an example of using the combined model to predict lifetime versus peak temperature during IOL, for four different EPC devices. All devices have BGA topology, and therefore the standard correlation fit exponent (n = –0.85) were used. Geometrical details about the bump layout are provided in the figure for reference. In all cases, the same basic IOL temperature profile was used (3-minute cycle period), and the total temperature change achieved during the cycle was adjusted (x-axis in the plot).

In the high temperature variation regime (right side of the graph), lifetime is strongly dependent on the solder geometry. The strain energy is dominated by global CTE mismatch, and the principal factors are the DNP and the standoff height of the solder bump. In the lower temperature regime, local mismatch becomes the dominant wear-out mechanism, and all devices converge to the same value. As ΔT moves toward 0, the lifetime grows rapidly, owing to strong non-linearity in the creep constitutive equation. This is good news for practical use cases involving small (< 10°C) temperature excursions, because all parts are expected to have lifetimes well above 1E6 cycles.

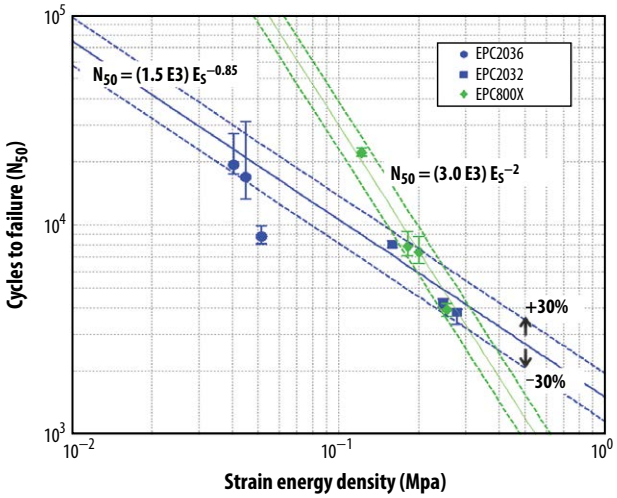
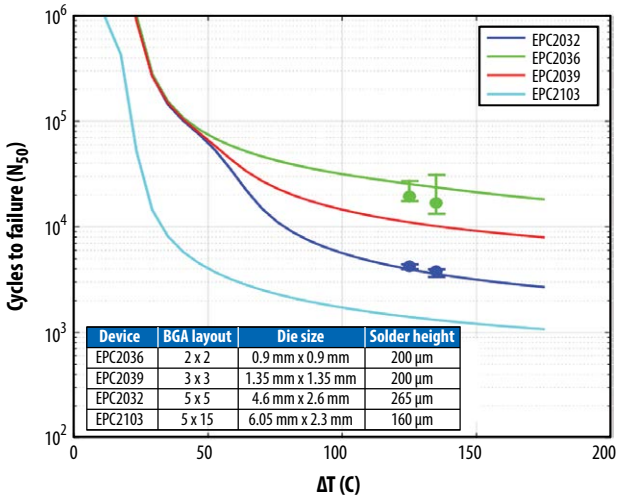


Figure 10. Correlation between cycles to failure and calculated strain energy density. EPC2036 & EPC2032 (BGA type) are fit to the blue line, with exponent near -1. EPC800x (LGA) follows a steeper line (green) with exponent of -2. Dashed lines indicate ± 30% from fit centerline.



Device	BGA layout	Die size	Solder height
EPC2036	2 x 2	0.9 mm x 0.9 mm	200 µm
EPC2039	3 x 3	1.35 mm x 1.35 mm	200 µm
EPC2032	5 x 5	4.6 mm x 2.6 mm	265 µm
EPC2103	5 x 15	6.05 mm x 2.3 mm	160 µm

Figure 11. Cycles to 50% Failure under IOL stress for four different EPC products, all having a BGA type pad layout. These calculations assume a 3-minute temperature profile (1-minute ramp up, 2-minute ramp down), with varying peak temperature change during the cycle (x-axis). These curves were generated by calculating the total strain energy density, and then using the correlation equation appropriate for BGA geometry. Where appropriate, measured cycles to failure data has been overlaid on the curves.

Figure 12 shows a similar exercise of the combined model, however this time the stress conditions are temperature cycling (TC) instead of IOL. A typical 1-hour cycle period was assumed, with 5-minute dwell at each temperature extreme. For TC, the lifetimes are lower compared to IOL for two main reasons: (1) the longer dwell at the temperature extremes allows for more creep flow and causes higher strain energy density; and, (2) the case and board are at the same temperature always, leading to slightly higher sheer stress in the joints.

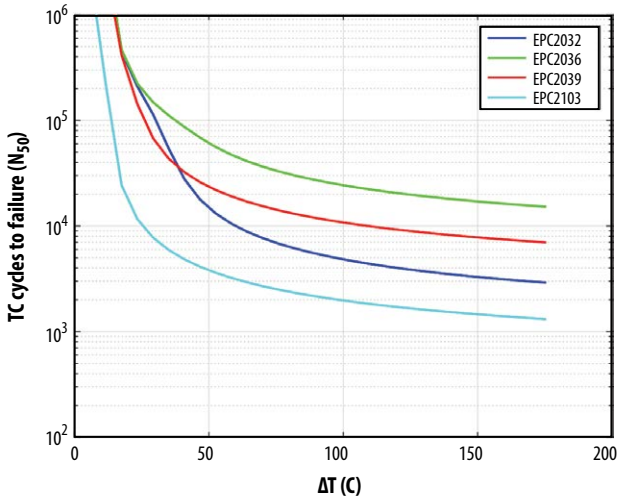


Figure 12. Cycles to 50% Failure under a TC stress for 4 different EPC products, all having a BGA type pad layout. These calculations assume a 60-minute temperature cycle, with varying peak temperature change during the cycle (x-axis). These curves were generated by calculating the total strain energy density, and then using the correlation equation appropriate for BGA geometry.

Future Work

To further validate and improve the fidelity of the combined thermo-mechanical model, the following activities are planned:

- Conducting additional IOL trials on selected BGA devices to verify correlation slope holds up against an expanded dataset
- Conducting additional IOL trials on LGA type devices, and study the correlation slope exponent for these non-regular solder layouts
- Improving simulation of strain energy density
  - Global Mismatch: Use finite elements to calculate global assembly stiffness parameter directly, without need for simplified spring model.
  - Identifying Local Mismatch: Use finite elements to capture the strain field (including biaxial and shear stress) in a solder ball. Hysteresis loops can be calculated within the FEM transient simulation.
- Logging temperature versus time for small die (e.g. EPC2036) under IOL. The changing case temperature resulting from increased $R_{\theta JB}$ at partially failed bumps, gives an opportunity to directly measure crack initiation and propagation rate during stress. It also allows for more accurate estimation of strain energy density, to account for the increase in die temperature as the IOL run progresses.

Summary

As described in this report, EPC continues to study the board level reliability of surface mount wafer level chip-scale packages used for eGaN FETs and ICs. A thermo-mechanical stress model is shown that combines knowledge from industry publications, EPC's own calculations, and actual stress test measurements of EPC devices. The result is a model that can be used to predict cumulative number of thermal cycles to failure, for an arbitrary stress temperature profile and die to PCB geometry. In addition, the fundamental methodology of how to compute the strain energy density at the solder joints during thermal stress is provided (see Appendix A). As described in the previous section, EPC will continue to refine the model with additional experiments to help customers integrate eGaN® FETs and ICs within their applications.

APPENDIX A: METHOD TO CALCULATE STRAIN ENERGY DENSITY

Strain energy was calculated using the methodology described by Clech in [26][27]. The method is summarized here, and the reader is referred to the original references for more details.

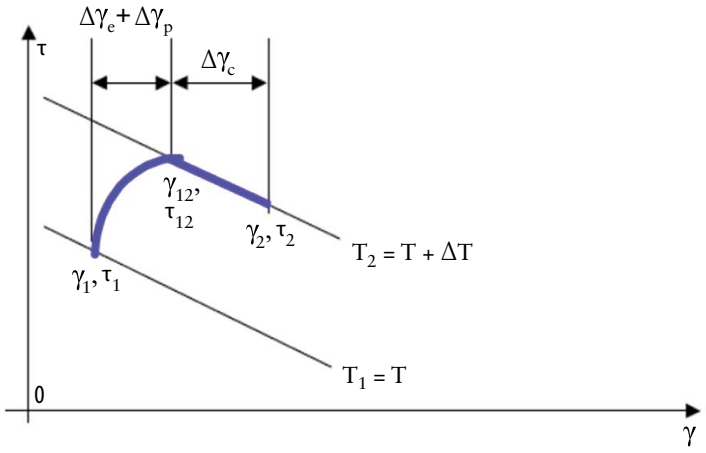


Figure 13. Schematic of a small-time step showing stress and strain in the joint as the temperature rises by ΔT. Taken from Ref [26].

The algorithm breaks the temperature cycle into a series of small time steps. In each step, the temperature changes by a small amount ΔT as prescribed by the temperature waveform. At the beginning of each step, the solder is in a certain shear stress-strain state denoted by (τ1 γ1). At the end of the step, the stress-strain (τ2 γ2) is calculated by solving four equations for four unknowns:

$$\gamma_{12} + \frac{\tau_{12}}{\kappa} = L_{DNP}\Delta\alpha\frac{(T2 - T0)}{h_s} \qquad \text{Eq. A1}$$

$$\gamma_{2} + \frac{\tau_{2}}{\kappa} = L_{DNP}\Delta\alpha\frac{(T2 - T0)}{h_s} \qquad \text{Eq. A2}$$

$$\gamma_{12} - \gamma_{1} = \frac{(\tau_{12} - \tau_{1})}{G\,(T1)} \qquad \text{Eq. A3}$$

$$\gamma_{2} - \gamma_{12} = \frac{d\gamma_{ss}}{dt}(T_2, \tau_{12}) \qquad \text{Eq. A4}$$

As shown in figure 13, the stress-strain change is treated as if it occurs in two discrete steps. In the first step, the stress-strain transitions from (τ1 γ1) to (τ12 γ12) via pure elastic deformation. This is captured in Eq. A3 above, where G(T1) is the temperature dependent elastic shear modulus of the solder. In the second step, the stress in the solder relaxes via creep deformation. This step is described by Eq. A4, where $d\gamma_{SS}/dt$ is the steady state creep rate. For this, we used the constitutive equation of Darveaux *et al* [25], which gives the steady state creep rate as a function of temperature (T in Kelvin) and stress level (σ):

$$\frac{d\gamma_{ss}}{dt} = C[\sinh(\alpha\sigma)]^n \exp\left(\frac{-Q_a}{kT}\right) \qquad \text{Eq. A5}$$

$$C = 5.77 \times 10^5 \left(\frac{1}{\text{sec}}\right)$$

$$\alpha = 0.045 \left(\frac{1}{\text{MPa}}\right)$$

$$n = 7.0$$

$$Q_a = 0.6\ (\text{eV})$$

The parameters appearing in Eq. A5 were taken from [25] appropriate for SAC305 type solder.

Eq. A1 and Eq. A2 express the constraint that, at any time during the cycle, the stress-strain must balance the shearing forces imposed by the thermal expansion mismatch between the board and package. In these equations, L_{DNP} is the distance to the neutral plane, Δα is the CTE mismatch between board and package, and h_s is the solder joint stand-off height. The parameter κ is the assembly stiffness constant, which considers the mechanical stiffness of the board and package. During a temperature change, some of the shear force can be dissipated by deformations in the board and package. For very stiff assembles (high κ), all of the shear force is taken up by strain in the solder joint.

Hysteresis loops are calculated by integrating stress-strain over an entire cycle, at each time step solving equations A1-A4 for (τ2 γ2) at the end of the step. In practice, multiple cycles (approximately 10) must be integrated before the hysteresis loops converge on a final closed loop. Once the final loop shape has converged, the strain energy density (area inside the loop) is calculated using the standard polygon area algorithm.

To account for the non-uniform temperature in the package and board during IOL stress, Clech's algorithm was adapted to create an effective ΔT_{eff} for use in Eq. A1 and Eq. A2.

$$\Delta T_{eff} = \frac{1}{(\alpha_c - \alpha_b)}\left(\alpha_c - \alpha_b\left(1 - \frac{\Theta_{jb}}{\Theta_{jb} + \Theta_{ja}}\right)\right)\Delta T \qquad \text{Eq. A6}$$

In the case of regular temperature cycling (TC), equations A1 and A2 can be used without modification.

Where α_b and α_c are the board and component CTE respectively, Θ_{jb} is the thermal resistance (in °C/W) from junction to board (from datasheet), and Θ_{ja} is the thermal resistance from board to ambient. This parameter depends on the heat sinking environment of the IOL test hardware in use; for EPC's hardware, the value was calibrated to be Θ_{ja} = 82°C/W.

The temperature dependent shear elastic modulus G (appearing in Eq. A3) for SAC305 solder was taken from the NIST database of lead-free solders [24]:

$$G(T) = a + bT + cT^2 \qquad \text{Eq. A7}$$

$$a = 20.24\ \text{GPa}$$

$$b = -2.635 \times 10^{-2}\left(\frac{\text{GPa}}{°\text{C}}\right)$$

$$c = -6.503 \times 10^{-5}\left(\frac{\text{GPa}}{°\text{C}}\right)$$

where T is the temperature (in Celsius).

Equations A1-A7 provide a full mathematical basis to calculate stress-strain hysteresis loops and strain energy density for EPC's wafer level chip-scale packages. The algorithm is not numerically intensive, and can be implemented in a variety of mathematical platforms, including Excel. MATLAB was used in this study and the code used can be provided to customers needing to do application specific computations.

APPENDIX B: PRODUCT QUALIFICATION STRESS TEST SUMMARY

EPC's eGaN® FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts were subjected to a drain-source voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts were subjected to a gate-source voltage at the maximum rated temperature
- High temperature storage (HTS): Parts were subjected to heat at the maximum rated temperature
- Temperature cycling (TC): Parts were subjected to alternating high- and low-temperature extremes
- High temperature high humidity reverse bias (H3TRB): Parts were subjected to humidity under high temperature with a drain-source voltage applied
- Unbiased autoclave (AC or Pressure Cooker Test): Parts were subjected to pressure, humidity, and temperature under condensing conditions
- Moisture sensitivity level (MSL): Parts were subjected to moisture, temperature, and three cycles of reflow.
- Electrostatic discharge (ESD): Parts were subjected to ESD under human body (HBM), machine (MM), and charged device (CDM) models.
- Intermittent operating life (IOL): Parts were subjected to an on/off cyclic DC power pulse, which heats the device junction to a predefined temperature, and subsequently to an off- state junction temperature.

The stability of the devices was verified with DC electrical tests after stress biasing. The electrical parameters were measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance were compared against the data sheet specifications. A failure was recorded when a part exceeds the datasheet specifications. eGaN® FETs were stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) standards [19] when possible. Parts were mounted onto FR5 (high Tg FR4) or polyimide adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top and inner copper layers were 1 oz. or 2 oz. Kester type 3 SAC305 or SAC405 solder [4] no clean flux was used in mounting the part onto an adaptor card.

Summary of Statistical Stress Results

Table 2 summarizes reliability tests results and provides a composite statistical estimator of the failure rate. A combined total of over nine million device-hours have been accumulated with zero failures. Since there are no failures, the statistic represents the worst case upper bound with 60% confidence.

These upper bound values are limited only by the sample size, and will continue to drop as EPC continues to collect reliability data. For some stress tests where appropriate, both failures in time (FIT) and mean time to failure (MTTF) was calculated. These calculations assume an acceleration factor (AF) = 1. Therefore, operating under less stringent use conditions will yield an even lower projected rate of failure. For other stress tests, the failure rate (in ppm) is provided, along with the associated stress time period.

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (hrs)	Upper Bound Failure Statistic (60% Confidence)	Notes
HTRB	2062	0	3063000	299 FIT (MTTF = 381 yrs)	$V_{DS} = 80\% V_{DS;max}$
HTGB	2079	0	3234000	283 FIT (MTTF = 402 yrs)	$V_{GS} \geq 5.5$ V
TC	1380	0	1585867	N/A	$\Delta T \geq 100°C$
H3TRB	708	0	708000	1294 FIT (MTTF = 88 yrs)	—
ELFR_HTRB	8366	0	401568	110 ppm	First 48 hrs
ELFR_HTGB	4833	0	231984	190 ppm	First 48 hrs
IOL	385	0	157850	N/A	—
All Tests	**19813**	**0**	**9382269**		

Table 2. Summary of Composite Upper Bound Failure Statistics .

High Temperature Reverse Bias

As part of the standard qualification samples were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [5]. The part types on stress testing covered the full voltage range of 40 – 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2023	30	XL (6.05 x 2.3)	T = 150°C, V_{DS} = 24 V	0	77 x 1	1000
HTRB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 40 V	0	77 x 3	1000
HTRB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC2014C	40	M (1.7 x 1.1)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC2024	40	XL (6.05 x 2.3)	T = 150°C, V_{DS} = 32 V	0	60 x 1	1000
HTRB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{DS} = 48 V	0	77 x 1	1000
HTRB	EPC2021	80	XL (6.05 x 2.3)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2029	80	XL (4.6 x 2.6)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2032	100	XL (4.6 x 2.6)	T = 150°C, V_{DS} = 80 V	0	77 x 2	1000
HTRB	EPC2001C	100	L (4.1 x 1.6)	T = 150°C, V_{DS} = 80 V	0	77 x 2	3000
HTRB	EPC2016C	100	M (2.1 x 1.6)	T = 150°C, V_{DS} = 80 V	0	77 x 3	2000
HTRB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 80 V	0	77 x 1	1000
HTRB	EPC2033	150	XL (4.6 x 2.6)	T = 150°C, V_{DS} = 120 V	0	77 x 2	1000
HTRB	EPC2034	200	XL (4.6 x 2.6)	T = 150°C, V_{DS} = 160 V	0	77 x 1	1000
HTRB	EPC2010C	200	L (3.6 x 1.6)	T = 150°C, V_{DS} = 160 V	0	77 x 2	3000
HTRB	EPC2012C	200	M (1.7 x 0.9)	T = 150°C, V_{DS} = 160 V	0	77 x 1	1000

Table 3. High Temperature Reverse Bias Test. Note: EPC800x results are applicable to all products in the EPC8000 series.

High Temperature Gate Bias

Parts were subjected to 5.75 V or 5.5 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [5]. The part types on stress testing covered the full voltage range of 40 – 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2023	30	XL (6.05 x 2.3)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{GS} = 5.5 V	0	77 x 3	1000
HTGB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	2000
HTGB	EPC2014C	40	M (1.7 x 1.1)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	2000
HTGB	EPC2015C	40	L (4.1 x 1.6)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	3000
HTGB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2021	80	XL (6.05 x 2.3)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2029	80	XL (4.6 x 2.6)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2032	80	XL (4.6 x 2.6)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2001C	100	L (4.1 x 1.6)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2016C	100	M (2.1 x 1.6)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	2000
HTGB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2038	100	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2033	150	XL (4.6 x 2.6)	T = 150°C, V_{GS} = 5.5 V	0	77 x 2	1000
HTGB	EPC2034	200	XL (4.6 x 2.6)	T = 150°C, V_{GS} = 5.75 V	0	77 x 1	1000
HTGB	EPC2010C	200	L (3.6 x 1.6)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2012C	200	M (1.7 x 0.9)	T = 150°C, V_{GS} = 5.75 V	0	77 x 1	1000

Table 4. High Temperature Gate Bias Test. Note: EPC800x results are applicable to all products in the EPC8000 series.

High Temperature Storage

Parts were subjected to heat at the maximum rated temperature, in accordance with JEDEC Standard JESD22-A103 [6].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2023	30	XL (6.05 x 2.3)	T = 150°C, Air	0	25 x 1	1000
HTS	EPC800x	40	S (2.05 x 0.85)	T = 150°C, Air	0	77 x 3	1000
HTS	EPC2021	80	XL (6.05 x 2.3)	T = 150°C, Air	0	25 x 1, 77 x 1	1000
HTS	EPC2029	80	XL (4.6 x 2.6)	T = 150°C, Air	0	25 x 3	1000
HTS	EPC2032	80	XL (4.6 x 2.6)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2022	100	XL (6.05 x 2.3)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2001C	100	L (4.1 x 1.6)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2016C	100	M (2.1 x 1.6)	T = 150°C, Air	0	77 x 2	1000

Table 5. High Temperature Storage Test.
Note: EPC800x results are applicable to all products in the EPC8000 series.

Temperature Cycling

Parts were subjected to temperature cycling between either (–40°C and +125°C) or (0°C and +100°C) for a total of 1000 cycles or 1500 cycles respectively, in accordance with JEDEC Standard JESD22-A104 [7].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2040	15	S (0.85 x 1.2)	–40 to +125°C, Air	0	32 x 1	1000
TC	EPC2023	30	XL (6.05 x 2.3)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2023	30	XL (6.05 x 2.3)	–40 to +125°C, Air	0	25 x 1	500
TC	EPC800x	40	S (2.05 x 0.85)	–40 to +125°C, Air	0	77 x 3	1000
TC	EPC800x	40	S (2.05 x 0.85)	–40 to +125°C, Air	0	35 x 1	1000
TC	EPC2021	80	XL (6.05 x 2.3)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2029	80	XL (4.6 x 2.6)	–40 to +125°C, Air	0	35 x 2, 77 x 1	1000
TC	EPC2021	80	XL (6.05 x 2.3)	–40 to +125°C, Air	0	77 x 1	500
TC	EPC2022	80	XL (6.05 x 2.3)	–40 to +125°C, Air	0	77 x 1	500
TC	EPC2032	100	XL (4.6 x 2.6)	–40 to +125°C, Air	0	77 x 2	1000
TC	EPC2001C	100	L (4.1 x 1.6)	–40 to +125°C, Air	0	35 x 3	1000
TC	EPC2107	100	S (1.35 x 1.35)	–40 to +125°C, Air	0	77 x 1	1000
TC	EPC2010C	200	M (3.6 x 1.6)	–40 to +125°C, Air	0	35 x 1	1000

Table 6. Temperature Cycling Test.
Note: EPC800x results are applicable to all products in the EPC8000 series.

Intermittent Operating Life

Parts were subjected to biased power cycling with junction temperature difference ≥ 100°C, in accordance with MIL-STD-750-1 [22].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
IOL	EPC800x	40	S (2.05 x 0.85)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 3	10000
IOL	EPC2001C	100	L (4.1 x 1.6)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 1	6000
IOL	EPC2032	100	XL (4.6 x 2.6)	Tj_off = +40°C, Tj_on = +140°C, delta_Tj = 100°C	0	77 x 1	5000

Table 7. Intermittent Operating Life Test.
Note: EPC800x results are applicable to all products in the EPC8000 series.

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias at 85% RH and 85°C under 49.1 PSIA vapor pressure for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A101 [8].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2023	30	XL (6.05 x 2.3)	T = 85°C, RH = 85%, V_{DS} = 24 V	0	77 x 1	1000
H3TRB	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	77 x 3	1000
H3TRB	EPC2015	40	L (4.1 x 1.6)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	50 x 1	1000
H3TRB	EPC2029	80	XL (4.6 x 2.6)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	25 x 1	1000
H3TRB	EPC2022	100	XL (6.05 x 2.3)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	50 x 1, 25 x 1	1000
H3TRB	EPC2032	100	XL (4.6 x 2.6)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 1	1000
H3TRB	EPC2001C	100	L (4.1 x 1.6)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 1	1000
H3TRB	EPC2016C	100	M (2.1 x 1.6)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 2	1000
H3TRB	EPC2033	150	XL (4.6 x 2.6)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	25 x 2	1000
H3TRB	EPC2010	200	L (3.6 x 1.6)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50 x 1	1000
H3TRB	EPC2012	200	M (1.7 x 0.9)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50 x 1	1000

Table 8. High Temperature High Humidity Reverse Bias Test.
Note: EPC800x results are applicable to all products in the EPC8000 series.

Autoclave (Unbiased Pressure Cooker)

Parts were subjected to 100% RH at 121°C under 29.7 PSIA vapor pressure for a stress period of 96 hours, in accordance with JEDEC Standard JESD22A-102 [9]. Devices were not electrically biased during stress.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
AC	EPC2001C	100	L (4.1 x 1.6)	T = 121°C, RH = 100%	0	25 x 1	96
AC	EPC2016C	100	M (2.1 x 1.6)	T = 121°C, RH = 100%	0	25 x 2	96

Table 9. Autoclave Test.

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Lead-free reflow in accordance with the IPC/JEDEC Joint Standard J-STD-020 [10].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	77 x 3	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168
MSL1	EPC2029	80	XL (4.6 x 2.6)	T = 85°C, RH = 85%, 3 reflow	0	25 x 2, 77 x 2	168
MSL1	EPC2032	80	XL (4.6 x 2.6)	T = 85°C, RH = 85%, 3 reflow	0	77 x 1	168
MSL1	EPC2001C	100	L (4.1 x 1.6)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168

Table 10. Moisture Sensitivity Level Test. Note: EPC800x results are applicable to all products in the EPC8000 series.

Electrostatic Discharge

Parts were subjected to ESD HBM, MM, and CDM in accordance with the JEDEC Standard JESD22A-114 [11] Human Body Model, JESD22A-115 [12] Machine Model, JESD22C-101 [13] Charged Device Model. EPC2001 and EPC800x were selected for the test to cover the die size range.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin G-S	(±) 400 V	(+) 500 V	1A
HBM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin G-D	(±) 1500 V	(-) 2000 V	1C
HBM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
MM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin G-S	(±) 200 V	(-) 400 V	B
MM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin G-D	(±) 400 V	(+) 600 V	C
MM	EPC2001	100	L (4.1 x 1.6)	Pin to Pin D-S	(±) 600 V	—	> Class C

Table 11. Electrostatic Discharge Test EPC2001.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001C	100	L (4.1 x 1.6)	Pin to Pin G-S	(±) 3000 V	(-) 4000 V	2
HBM	EPC2001C	100	L (4.1 x 1.6)	Pin to Pin G-D	(±) 2000 V	(-) 3000 V	2
HBM	EPC2001C	100	L (4.1 x 1.6)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
CDM	EPC2001C	100	L (4.1 x 1.6)	Pin to Pin - All Pins	(±) 1000 V	—	C3

Table 12. Electrostatic Discharge Test EPC2001C.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 350 V	(-) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 350 V	(+) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 500 V	(+) 1000 V	1B
CDM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin - All Pins	(±) 500 V	(-) 500 V	1C
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 25V	(+) 50 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 100 V	(-) 200 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 50 V	(+) 100 V	A

Table 13. Electrostatic Discharge Test EPC800x Note: EPC800x results are applicable to all products in the EPC8000 series.

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